Architecting NP-Dynamic Skybridge

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Abstract—This paper introduces a new fine-grained 3D IC fabric technology called NP-Dynamic Skybridge. Skybridge is a family of 3D IC technologies that provides fine-grained vertical integration. In comparison to the original 3D Skybridge, the NP-Dynamic approach enables a more comprehensive logic style for improved efficiency. It addresses device, circuit, connectivity and manufacturability requirements with an integrated 3D mindset. The NP-Dynamic 3D circuit style enables wide range of logic expressions, simple clocking scheme, and reduces buffer requirements. Architected interconnect framework in 3D provides a high degree of connectivity. Bottom-up evaluations for 16-nm NP-Dynamic Skybridge, considering material properties, nanoscale transport, 3D circuit style, 3D placement and layout reveal up to 50x density and 25x power benefits for 4-bit CLA in comparison to 16-nm CMOS at comparable performance. For 4-bit multiplier, NP-Dynamic Skybridge shows up to 90x density benefit and 8x lower power vs. CMOS.

Index Terms—3D IC fabric, NP-Dynamic circuits, emerging technologies, vertical nanowires, nanoscale computing fabrics

I. INTRODUCTION

With the transition of technology nodes to nanoscale, CMOS faces severe challenges that result from device scaling limitations [2][3], interconnection bottlenecks [4] and increasing manufacturing complexities [4]. To continue scaling, a fine-grained 3D integrated circuit fabric, called Skybridge [1], was proposed that addresses nanoscale challenges while achieving orders of magnitude benefits over CMOS. In Skybridge, core aspects from device to circuit style, connectivity, thermal management and manufacturing pathway are co-architected in a 3D fabric-centric manner. This mindset offers several pathways to physically implement fine-grained 3D ICs. The original Skybridge uses uniform n-type transistors in a dynamic circuit style, where NAND and AND-of-NAND compound gates are elementary logic functions. Cascading of logic stages requires multiple clock signals to avoid signal monotonicity problem, and buffers are used in between stages for signal propagation and restoration in large-scale designs.

In this paper, we propose a different approach incorporating both n- and p-type transistors to build a new class of fine-grain 3D circuits, called NP-Dynamic Skybridge, which expands on the degree of flexibility in expressing logic functions for improved efficiency. Similar to original Skybridge, NP-Dynamic Skybridge follows a fabric-centric mindset, where architectural and design choices are optimized at physical fabric level for 3D compatibility. Due to the unique integration approach and design choices, nanoscale challenges are solved, and significant benefits are attained over 2-D CMOS. The NP-Dynamic Skybridge fabric based designs even show improvements over original Skybridge while still maintaining 3D compatibility and manufacturability. In this fabric, both n- and p-type transistors are used in a NP-Dynamic circuit style, where n- and p-type dynamic logic gates are cascaded to avoid monotonicity problem. This allows a wide range of elementary logic functions to be supported including NAND, AND-of-NAND, NOR and OR-of-NOR, which provide flexibility for circuit design, and allow compact circuit implementations. In addition, it simplifies clocking scheme, and reduces number of buffers for large-scale designs.

Our comprehensive fabric evaluation for the example arithmetic circuits designed, accounting for nanoscale materials, device, 3D circuit style, 3D placement and 3D layout, indicates tremendous benefits in comparison to 16-nm CMOS. In particular, 4-bit CLA shows up to 50x density benefit and 25x lower power at comparable performance, and 4-bit multiplier shows up to 90x higher density with 8x lower power than CMOS. The NP-Dynamic Skybridge based designs also show improvement over original Skybridge design; our evaluations show 2x density and 2x power efficiency in comparison to original Skybridge for equivalent 4-bit CLA design at 16nm. Fabric features can be architected for thermal management similar to original Skybridge, and bottom-up manufacturing flow can be used that primarily relies on material deposition techniques for active component formation [1].

The key contributions of this paper are: (i) details of NP-Dynamic Skybridge fabric, its core components and circuit style are presented; (ii) extensive characterization of architected core components: n- and p-type Vertical Gate-All-Around (V-GAA) junctionless transistors and Ohmic contact structure are shown; and (iii) a comprehensive bottom-up simulation methodology is presented, and used for evaluating and benchmarking arithmetic circuits with respect to original Skybridge and 2-D CMOS in 16nm technology node.

The rest of the paper is organized as follows: Section II presents the proposed new fabric's core components. In Section III, we show how to build elementary circuits based on the core components. Section IV shows the simulation methodology of the proposed fabric. Section V shows the benchmarking results, and Section VI concludes the paper.
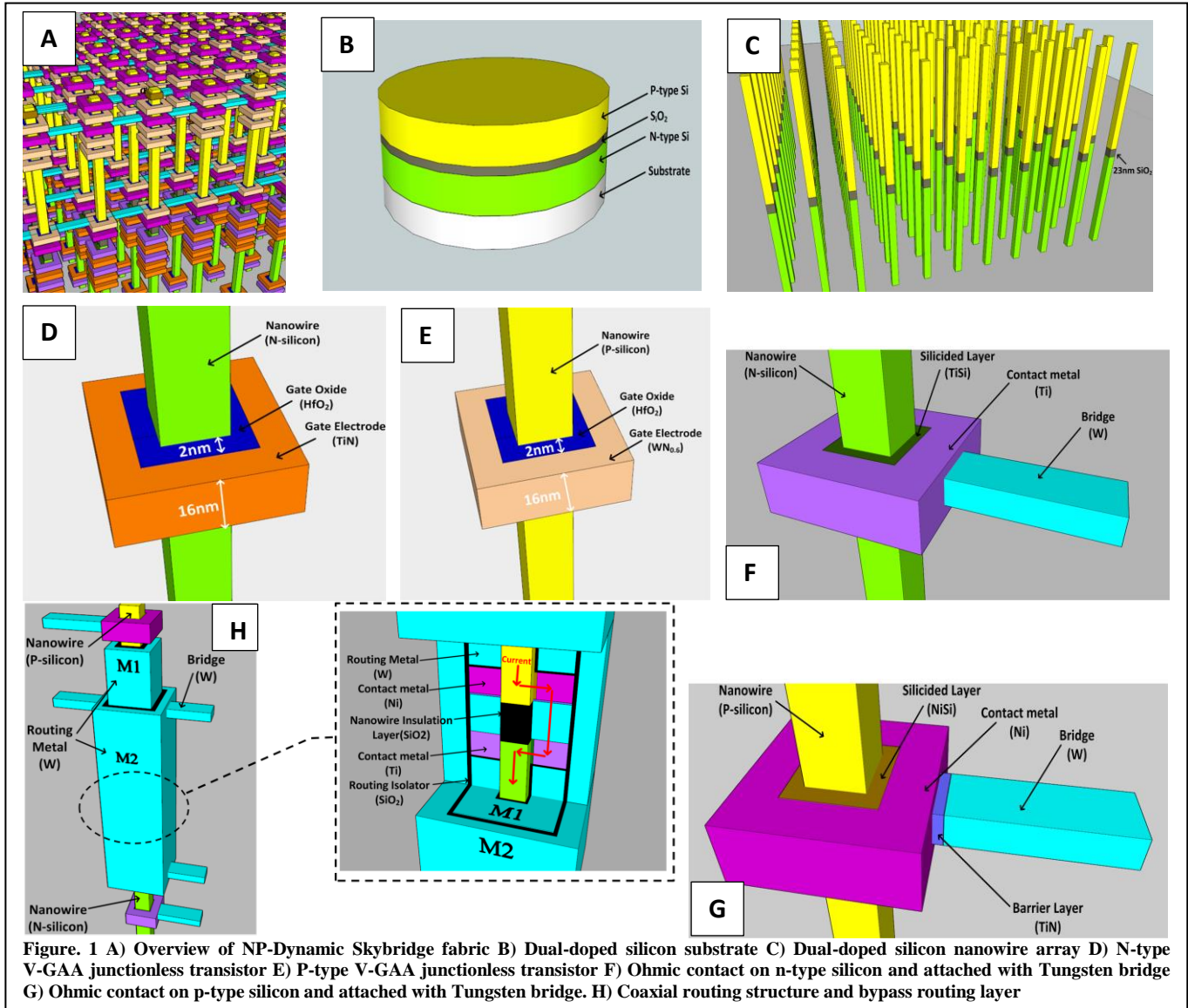
Figure. 1 A) Overview of NP-Dynamic Skybridge fabric B) Dual-doped silicon substrate C) Dual-doped silicon nanowire array D) N-type V-GAA junctionless transistor E) P-type V-GAA junctionless transistor F) Ohmic contact on n-type silicon and attached with Tungsten bridge G) Ohmic contact on p-type silicon and attached with Tungsten bridge. H) Coaxial routing structure and bypass routing layer

II.   CORE COMPONENTS

NP-Dynamic Skybridge design follows a fabric-centric mindset by assembling structures on a 3D uniform template of single crystal vertical nanowires, keeping 3D compatibility and overall efficiency as its central goal.

The envisioned NP-Dynamic Skybridge is shown in Fig. 1 A; nanowires are the core building blocks, and architected components are constructed on these nanowires primarily through material deposition techniques, similar to the process flow described in ref. [1]. Core architected components are: uniform dual-doped vertical nanowires, n- and p-type V-GAA junctionless transistors, Ohmic contacts connecting different doped regions, Coaxial routing structures and nanowire connecting bridges. In this section, we present the core components of this new fabric and illustrate how it is used in unison to achieve desired functionality.

A. Vertical Nanowires

As mentioned earlier, regular array of single crystal vertical silicon nanowires are fundamental building blocks;

these nanowires can be used as– (i) logic nanowires that use stacked transistors to implement required functionality, and (ii) routing nanowires for signal routing. The nanowire formation step precedes all manufacturing steps, and is done after wafer preparation. The wafer can be prepared by bonding heavily doped n-type and p-type substrates using techniques that are similar to the ones described in refs. [7][8]. Fig. 1B illustrates the wafer with both n-and p-type doped silicon layers which are vertically stacked. Between the n-type and p-type doped silicon layers, there is a silicon dioxide layer for isolation. Fig. 1C shows the dual-doped silicon nanowire with high aspect ratio which has p-type doped silicon on top half and n-type doped silicon region on bottom half; these nanowires can be patterned using both inductively coupled plasma etching, and oxidation and removal techniques [1].

B. Vertical Gate-All-Around Transistor

V-GAA junctionless transistors are used as active devices, and are formed on nanowires through consecutive material deposition steps. V-GAA junctionless transistors use uniform doping with no abrupt variation in Drain/Source/Channel regions that simplifies manufacturing requirements, and is especially suitable for this fabric. Fig. 1D and Fig. 1E show the structures of both n- and p-type transistors. Both of them are V-GAA junctionless transistors whose channel conduction is modulated by the workfunction difference between the heavily doped channel and the gate [9]. Titanium Nitride (TiN) and Tungsten Nitride (WN) are chosen for n-type and p-type transistors respectively to provide proper workfunction [10][11]. 3D TCAD Process [22] and Device simulations [22] were used to extract the device characteristics, shown in Fig. 2. The n-type device had an ON current of $30\,\mu A$, and OFF current 0.1nA. The p-type device had an ON current of $26\,\mu A$, OFF current 0.76nA. The simulation methodology is presented in Section IVA.
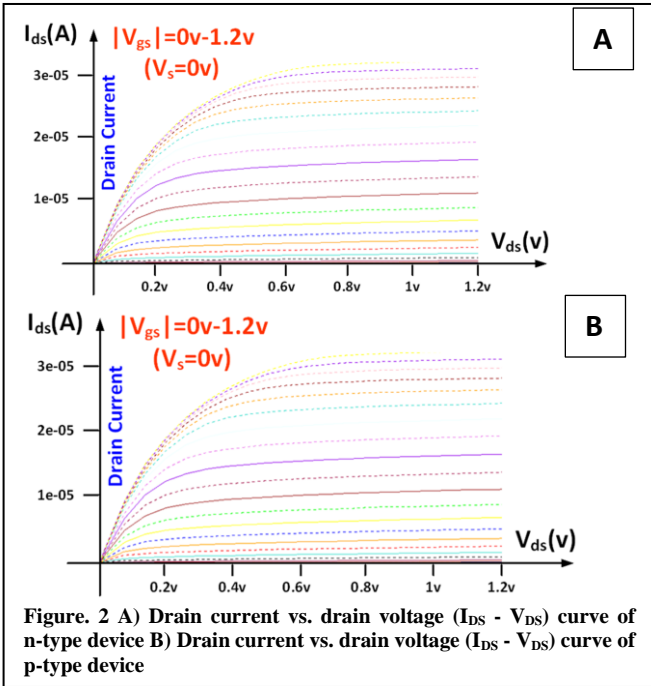

Figure. 2 A) Drain current vs. drain voltage (I_{DS} - V_{DS}) curve of n-type device B) Drain current vs. drain voltage (I_{DS} - V_{DS}) curve of p-type device

C. Ohmic Contacts

In NP-Dynamic Skybridge, low-resistance contacts are used to carry signals between heavily doped silicon and metal. To ensure low resistance contacts, specific materials are chosen for each doped regions (Fig. 1F and Fig. 1G). Nickel is used for p-type Ohmic contact and Titanium is chosen for n-type. Each of these metals has proper workfunction to form low Schottky Barrier with corresponding doped silicon, achieving low resistance; in addition, they also have good adhesion to doped silicon [13][14]. A thin Titanium Nitride layer in the p-type nanowire Ohmic contact is used for avoiding the reaction between Nickel and Tungsten.

D. Bridges

Bridges (Fig. 1F and Fig. 1G) connect with Ohmic contacts and coaxial routing structures to carry and propagate signals horizontally between input and output nodes. As shown in Fig. 1F and Fig. 1G, Tungsten is used as the material to form the bridges because of its good adhesion ability with Titanium [14].
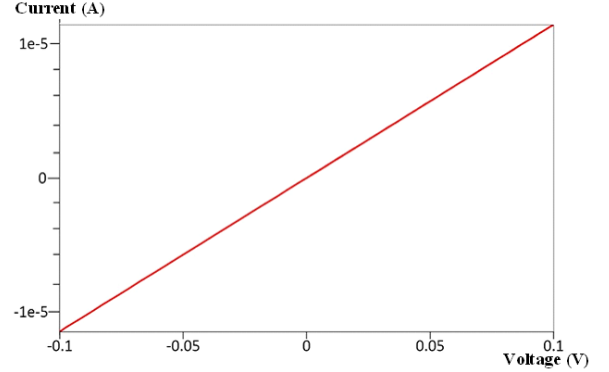

Figure. 3 I-V curve of the contact structure

E. Coaxial Routing Structures

Coaxial routing refers to a routing scheme, where a signal routes coaxially with another inner signal without affecting each other. The coaxial routing structure is used for routing in vertical direction, and to propagate signals between n- and p-doped regions. This is unique and enabled by the fabric's vertical integration approach, and can be manufactured similar to the process flow used in ref. [1]. Each coaxial structure (Fig. 1H) is built with two concentric metal layers separated by dielectric layers around a nanowire. A contact layer is formed around the nanowire to form low resistance Ohmic contact for signals to bypass the isolation layer between the n- and p-doped regions (Fig. 1H). Fig. 3 shows the I-V characteristics of the contact structure that was carried out by emulating the fabrication process flow in Synopsys Sentaurus Process and Device simulator [22] (See Section IVB). The resistance was found to be 5kΩ.

III. ELEMENTARY CIRCUITS

A. NAND/NOR Gate

Elementary logic gates such as NAND and NOR can be realized on a nanowire by stacking n- and p- type transistors respectively on the dual-doped nanowire. Fig. 4A and Fig. 4B show 5-input NAND and NOR gate implementations respectively. The benefits of 3D integration are obvious from Figs. 4A and 4B, where 7 transistors and 3 contacts occupy only one nanowire area footprint for NAND and NOR gate implementations. The use of p-type transistors also provides benefits over original Skybridge fabric for logic implementation. For example, building a 5-input NOR gate in original Skybridge fabric requires five 1-input NAND gates (5 nanowires); the outputs of these five NAND gates are then connected to realize AND-of-NAND logic to implement a NOR logic function. By contrast, NP dynamic Skybridge fabric uses only one p-type nanowire for NOR function. Thus NP-Dynamic Skybridge fabric offers higher design flexibility that can enable significant density, power and performance improvements over 2-D CMOS and original Skybridge.
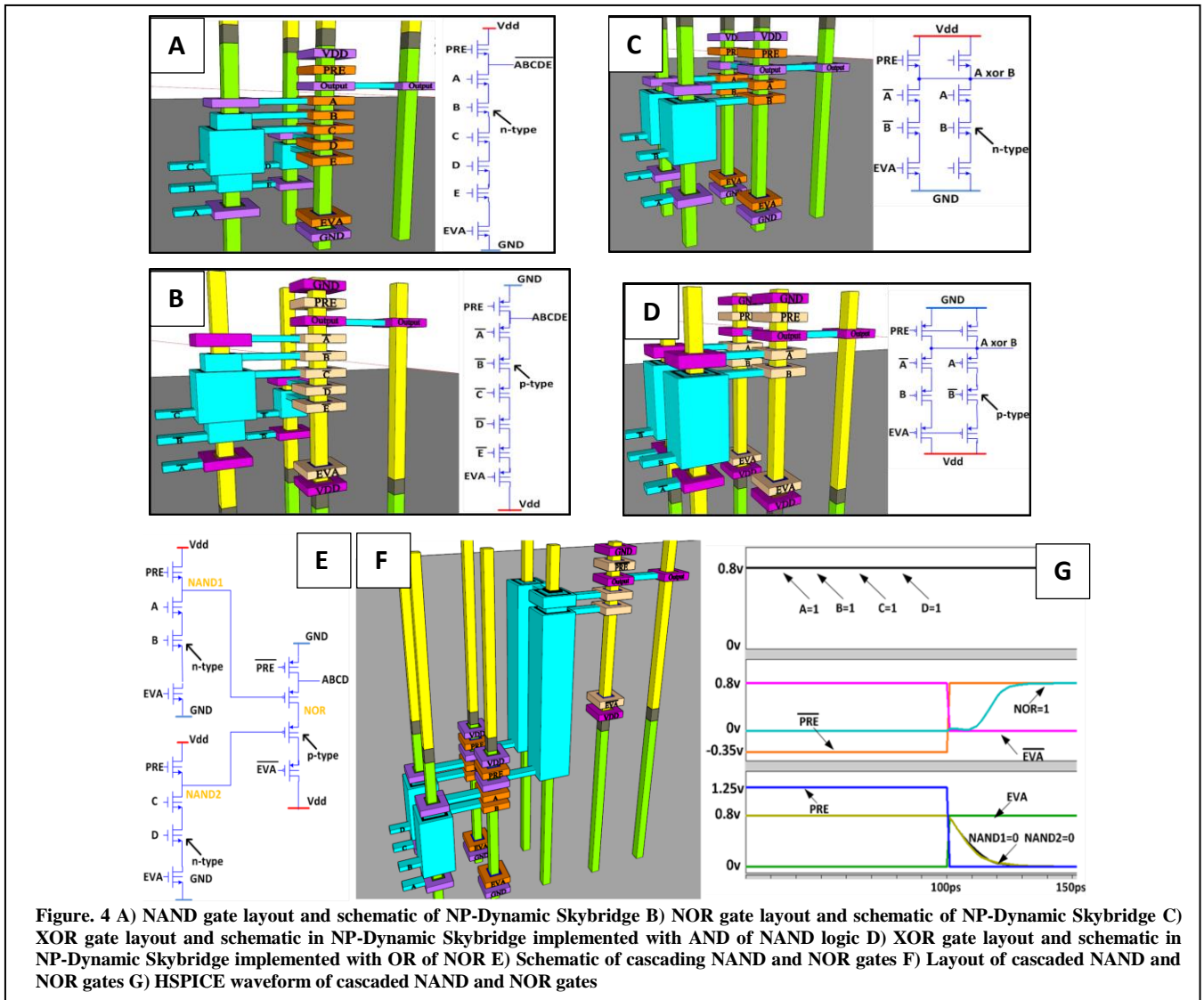
Figure. 4 A) NAND gate layout and schematic of NP-Dynamic Skybridge **B)** NOR gate layout and schematic of NP-Dynamic Skybridge **C)** XOR gate layout and schematic in NP-Dynamic Skybridge implemented with AND of NAND logic **D)** XOR gate layout and schematic in NP-Dynamic Skybridge implemented with OR of NOR **E)** Schematic of cascading NAND and NOR gates **F)** Layout of cascaded NAND and NOR gates **G)** HSPICE waveform of cascaded NAND and NOR gates

As shown in Figs. 4A and 4B, these elementary gates are controlled with *precharge* and *evaluate* clock signals. The NAND gate operates in the similar way as shown in original Skybridge [1]. For the NOR gate, the output node gets discharged during the *pre-discharge* phase, and the output is pulled up to a final value depends on the ON/OFF status of p-type transistors during the *evaluation* phase. As explained in ref. [6], n-type dynamic logic (NAND gate) requires monotonically rising signals as input while p-type dynamic logic (NOR gate) requires monotonically falling signals as input. Otherwise, monotonicity problem would happen during the *evaluation* phase.

B. Compound Gate

In addition to elementary Boolean gates, complex logic functions can also be designed in a single gate by using a combination of NAND/NOR gates. OR-of-NORs (/AND-of-NANDs) logic can be implemented by shorting the outputs of a collection of NOR (/NAND) gates; this is in contrast to original Skybridge, where only AND-of-NANDs logic is used. Fig. 4C and Fig. 4D illustrate an example, where an XOR gate is built by AND-of-NANDs and

OR-of-NORs logic respectively. These choices provide a higher degree of flexibility in circuit design.

C. Cascaded Gates

Cascading multiple logic gates is important for large-scale designs. In NP-Dynamic Skybridge, successive cascaded stages are alternately implemented using n- and p-type dynamic logic. This solves the signal monotonicity problem in cascading dynamic logic gates, and allows cascaded stages of a given circuit to be evaluated in the same clock period. Only one set of *precharge* and *evaluate* clocks is required. which results in simplified clocking scheme. The schematic diagram in Fig. 4E shows an example of cascaded gates. It was designed with two 2-input NAND gates in the first stage, followed by one 2-input NOR gate. The output of NAND gate was used to gate a NOR gate in the following stage. Fig. 4G shows the simulation output from HSPICE for functional validation. Initially, NAND gate output was *precharged* to logic 1 and NOR gate output was *pre-discharged* to logic 0 simultaneously. During the *evaluation* period, the evaluation of both NAND and NOR gates can be executed in the same clock phase because the NAND output provides

monotonically falling signal to the following NOR gate as input. The monotonically falling signal is the required input signal for p-type dynamic logic gate and allows cascaded dynamic logic gates.

The 3D layout of the above design is shown in Fig. 4F; three logic nanowires are used for implementing NAND and NOR logic gates, and three additional nanowires are used for input/output routing.

IV. METHODOLOGY

A. Device Simulations

The n-type and p-type V-GAA junctionless transistors were extensively characterized using accurate physics-based 3D simulation of the electrostatics and operations using Synopsys Sentaurus TCAD [22]. Gate material work function is 5.2eV (TiN) and 4.3eV (WN) for n-type and p-type transistors respectively [26]. 16nm channel length was simulated following similar feature size as original Skybridge's device. Uniform doping for drain, channel and source was required to form the V-GAA junctionless transistor, and As and Br were chosen as dopants for n- and p-type devices respectively. The doping concentration for n-type device was 10^{19} cm^{-3} and n-type was 10^{20} cm^{-3}. A high-k dielectric, HfO$_2$, was used for gate oxide. The gate oxide thickness was 3nm. Drift-diffusion model transport models were used to simulate the 3D V-GAA junctionless devices. Simulations were calibrated to account for interface scattering, surface roughness and interface trapped charges as explained in [1][24].

Drain current vs. drain voltage (I$_{DS}$ - V$_{DS}$) and capacitance vs. gate voltage (C vs. V$_{GS}$) characteristics were simulated (Fig. 4A-B). These simulations verify both accumulation mode behavior and depletion mode behavior for the devices when applied with a varied gate voltage.

B. Contact Structure Simulations

The silicon-metal contact interface, where there is a resistive interface region caused by Schottky Barrier of the interface between doped silicon and metal, was simulated with accurate physics-based 3D simulation of the electrostatics and operations using Synopsys Sentaurus TCAD. Fig. 5 shows the simulated contact structure that includes the interface between Nickel and p-type doped silicon, and the interface between Titanium and n-type doped
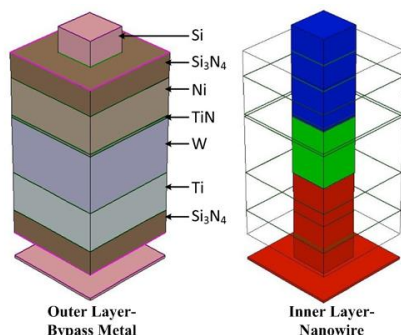
silicon. The area of each interface region is equal to the area of each contact in the bypass routing structure shown in Fig. 1G. The doping concentration was 10^{19} cm^{-3} for n-type silicon and the p-type silicon was doped with 10^{20} cm^{-3} concentration. The work function was defined 4.7eV for Nickel and 5.2 eV for Titanium [26]. The Schottky boundary model was chosen as physics model of the contact interface. Simulations were calibrated to account for interface scattering, surface roughness and interface trapped charges.

C. Circuit-level Simulations

Novel nanoelectronic devices do not have built-in models in traditional circuit simulators such as HSPICE [23]. Therefore, device simulation data were used to create behavioral models for the V-GAA junctionless devices compatible with HSPICE as explained in [25]. The behavioral models incorporate mathematical expressions for device current as a function of V$_{GS}$ and V$_{DS}$, and piecewise linear approximations of parasitic capacitance vs. V$_{GS}$.

The resistance and capacitance of interconnects were modeled using Predictive Technology Model (PTM) [16] and extracted from manually built 3D layout, which is designed based on original Skybridge design rules [1]. With the help of behavioral models and modeled interconnect RC values, HSPICE simulations were carried out to verify functionality and measure the performance and power for designs based on NP-Dynamic Skybridge fabric.

D. Area Evaluation

The example circuits used for benchmarking were designed and physical 3D layout was manually performed. Area footprint of each design was calculated based on the number of nanowires used and nanowire pitch as per Skybridge design rules [1].

V. BENCHMARKING AND RESULTS

Carry look-ahead adder and Array Based Multiplier [15] were used to evaluate NP-Dynamic Skybridge and compare with CMOS. Block diagrams of 4-bit CLA (3 stages) and 4-bit Array Based Multiplier (7 stages) are shown in Fig. 6B and Fig. 6A respectively. Each of them is implemented with NP-Dynamic circuit style described earlier. All stages finish the evaluations in one clock period, without the need for additional buffers for signal propagation.

Table II and III show the CLA and multiplier benchmarking results for NP-Dynamic Skybridge fabric, original Skybridge 3D fabric and CMOS at 16nm. NP-Dynamic Skybridge's 4-bit CLA design show 50x benefits of density and 25x power efficient in comparison to CMOS and the 4-bit multiplier design has 90x density benefits and 8x power efficiency compared with 16nm CMOS design. In comparison to original Skybridge's dual-rail based designs that are optimized for higher performance, NP-Dynamic's single-rail based both CLA and multiplier design achieve up to 2x power efficiency and 2x density benefits with comparable performance (original Skybridge's throughput is 10% better). Key factors contributing to degradation of throughput in NP-Dynamic Skybridge's designs are usage of fewer stages for pipelining,

Figure. 5 Simulated contact structure with p+ silicon, Nickel, Titanium, n+ silicon

and increased evaluation clock period compared to original Skybridge circuits.

$P_i = A_i \oplus B_i = \overline{(\overline{A_i} + B_i)} + \overline{(\overline{B_i} + A_i)}$ $G_i = \overline{(\overline{A_i + \overline{B_i}})}$

$\overline{C_i} = \overline{G_{i-1}} \cdot \overline{P_{i-1} C_{i-1}}$ $\overline{S_i} = C_i \otimes P_i = \overline{(\overline{C_i} \cdot P_i)} \cdot \overline{(\overline{P_i} \cdot C_i)}$

Figure. 6 (A) Block diagram of 4-bit array based multiplier in NP-Dynamic Skybridge fabric; (B) Block diagram of 4-bit CLA in NP-Dynamic Skybridge fabric
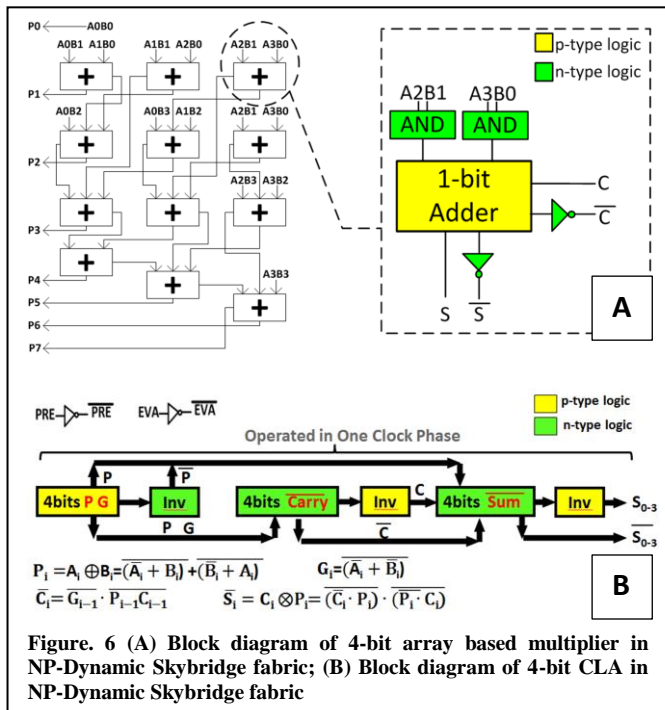
Table II Benchmarking Results 4-bit CLA

4-bit CLA	Latency (ps)	Power (uW)	Area (um²)	Throug-hput (Ops/s)	Throug-hput/ Power (Ops/J)
Skybridge (Dual-Rail)	100	22.0	0.76	10E+9	4.7E+14
NP-Dynamic Skybridge	50	9.5	0.36	8.8E+9	6.9E+14
CMOS	102	235	18.7	9.9e9	0.42E+14

Table III Benchmarking Results of 4-bit Multiplier

4-bit MULT	Latency (ps)	Power (uW)	Area (um2)	Throug-hput (Ops/s)	Throug-hput/ Power (Ops/J)
Skybridge (Dual-Rail)	457	42.3	1.27	5.1e9	1.2E+14
NP-Dynamic Skybridge	93	21.1	0.54	4.5e9	1.7E+14
CMOS	200	172	50	5.0e9	0.3E+14

VI. CONCLUSION

In this paper, we detailed a new vertical nanowire based 3D integrated circuits fabric called NP-Dynamic Skybridge. Fabric's core components and their comprehensive evaluations were shown. NP-Dynamic Skybridge expands on the original Skybridge fabric by offering a wide range of logic design choices, due to the use of both n- and p-type transistors. Our evaluations based on a bottom-up simulation methodology indicated significant benefits over CMOS for several arithmetic circuits. For example, our results show 90x density benefits and 8x power benefits for a 4-bit multiplier in comparison to CMOS at 16nm. Benefits were also attained with respect to original Skybridge; it achieves up to 2x power

efficiency and 2x density benefits for both 4-bit CLA and 4-bit multiplier design at 16nm. We expect that these benefits will scale to even larger designs, paving a new path for 3D ICs. Further work is ongoing which includes design and evaluation for large-scale circuits, and exprimental prototype.

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